Parylene-C passivated carbon nanotube flexible transistors

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Carbon nanotubes are extremely sensitive to the molecular species in the environment and hence require a proper passivation technique to isolate them against environmental variations for the realization of reliable nanoelectronic devices. In this paper, we demonstrate a parylene-C passivation approach for CNT thin film transistors fabricated on a flexible substrate. The CNT transistors are encapsulated with 1 and 3 μm thick parylene-C coatings, and the transistor characteristics are investigated before and after passivation. Our findings indicate that thin parylene-C films can be utilized as passivation layers for CNT transistors and this versatile technique can be readily applied for the encapsulation of CNT devices such as field effect transistors, p-n diodes, and logic circuits fabricated on flexible substrates. © *2010 American Institute of Physics*. [doi:10.1063/1.3499758]

Single-walled carbon nanotubes (SWNTs) with their unique physical, electrical, and mechanical properties are being considered as a potential replacement for existing semiconducting materials in flexible electronics. Their mobility can exceed 10^5 $cm^2/V\ s^{-1}$, and they have large current carrying (10^9 A/cm^2) capability, higher ON/OFF ratios ($>10^5$) and extreme mechanical flexibility.[1] SWNT based field effect transistors (FETs) exhibit p-type behavior in the ambient environment, and they can be converted to n-type by doping e.g., polymer functionalization.[2] Carbon nanotube (CNT) flexible devices such as high frequency FETs, p-n diodes, and logic circuits have already been reported.[3] Their large surface area to volume ratios and extreme sensitivity to the molecular species in the environment (e.g., oxygen, moisture, etc.) can significantly affect the electrical properties of CNT transistors.[4–6] To isolate SWNT based flexible transistors from environmental factors, thin and flexible passivation layers need to be investigated prior to deployment of these devices in real world applications.

Several groups have already explored passivation of CNT based devices with thin polymeric films yet had limited success. For example, Dai *et al.*[5] have reported a 1.7 μm polymer [polymethyl-methacrylate (PMMA)] coating for passivating CNT based transistors. When the PMMA encapsulated devices were exposed to a humid ambient, the electrical characteristics of the transistors changed due to permeation of water molecules through PMMA. Similarly, Zhang *et al.*[7] used SU-8/PMMA (2 μm/200 nm) to passivate their CNT FETs. After exposing their devices to an NO_2 environment for 1 h, they have noted that the gas molecules diffused through the SU-8/PMMA layer and caused variations in the transistor behavior. In addition to polymeric encapsulants, Kaminishi *et al.* and Kim *et al.*[8] have used Si_3N_4 (50 nm catalytic chemical vapor deposited at 270 °C) and Al_2O_3 (15 nm deposited using atomic layer deposition (ALD) at 300 °C) layers as passivation layers for CNT FETs. The drawback with both Si_3N_4 and ALD based deposition methods is that both materials are either deposited at or require annealing steps at elevated temperatures which limit their applications for flexible devices.

To realize flexible CNT FETs which are insensitive to environmental variations, high quality and thin encapsulation layers are needed which preserve the characteristics of the transistors, maintain their flexibility and at the same time possess good barrier properties. In this paper, we demonstrate a parylene-C passivation technique for CNT based thin film transistors which can be readily utilized for devices made on flexible substrates. Parylene-C is a pin hole free material, and can provide a uniform conformal coating over all surfaces regardless of the configuration of the surface (e.g., sharp edges and holes). It is also chemically inert, and has high dielectric strength and low permeability to moisture and gases. Film deposition is stress-free (deposited at room temperature), hence it does not introduce any adverse effects to the encapsulated devices. These attractive properties make parylene-C a promising encapsulation layer for flexible CNT based thin film transistors. We first fabricate CNT FETs on a flexible parylene-C substrate. After measuring the electrical characteristics of the CNT FETs, we next encapsulate the devices with thin (1 and 3 μm) parylene-C layers and study the characteristics of the devices before and after encapsulation.

A three-dimensional (3D) schematic of the fabrication process for flexible SWNT thin film transistors (TFTs) is shown in Fig. 1(a). First, a 10 μm thick parylene-C layer was deposited on an oxidized (500 nm) silicon wafer at room temperature. Parylene-C has a high tensile strength of 70 MPa and Young's modulus of 3.2 GPa (Ref. 9) which make it a promising material as a flexible substrate.[10,11] Next, aluminum gate electrodes (1500 Å) were sputter deposited and patterned using conventional optical lithography and wet etching. Then, a 1 μm thick parylene-C gate dielectric layer

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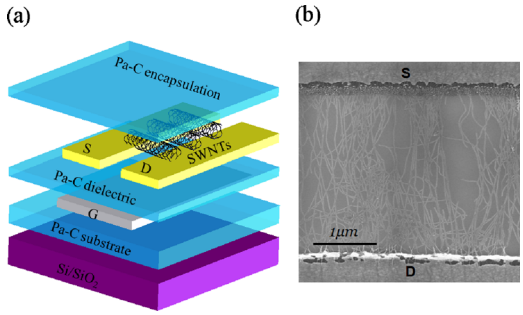

FIG. 1. (Color online) (a) A 3D schematic drawing of the bottom gated SWNT TFT, and (b) the high resolution SEM micrograph of assembled SWNTs between the source and drain electrodes.

was deposited. Subsequently, source and drain electrodes (Cr/Au, 5/150 nm) were sputter deposited and patterned by wet etching. SWNTs were next assembled across the source and drain electrodes by utilizing the dielectrophoretic (DEP) assembly process at 2 V_{pp} and 10 MHz for 1 min at room temperature [Fig. 1(b)]. After assembling the SWNTs, the electrical properties of the transistors were improved by reducing the metallic SWNTs from the channel via current induced electrical breakdown process.[12] Finally, a parylene-C passivation layer was deposited, and contact pads for probing were opened by etching parylene with oxygen plasma in an inductively coupled plasma etcher. Photoresist was used as a mask to etch the parylene-C layers. The detailed information of parylene-C deposition and patterning is described in our previous paper.[13]

After DEP assembly and the electrical burning breakdown process, we next measured the I-V characteristics of the transistors using a semiconductor parameter analyzer (HP4155A) at ambient room temperature and atmospheric pressure. After encapsulation, the electrical properties of the CNT FETs were remeasured and compared with the values obtained before encapsulation. Figures 2 and 3 summarize the transfer characteristics of these devices before and after parylene-C passivation. To preserve the flexibility of the devices, thinner coating layers are preferred since the rigidity of a flexible film is proportional to the cube of its thickness.[10] In our study, we used parylene-C films with two different thicknesses (1 and 3 μm). Both devices [Figs. 2 and 3] displayed a significant gate hysteresis before and after passivation between forward (V_{GF}) and backward (V_{GB}) sweeps of the gate voltage. This phenomenon is often observed in CNT

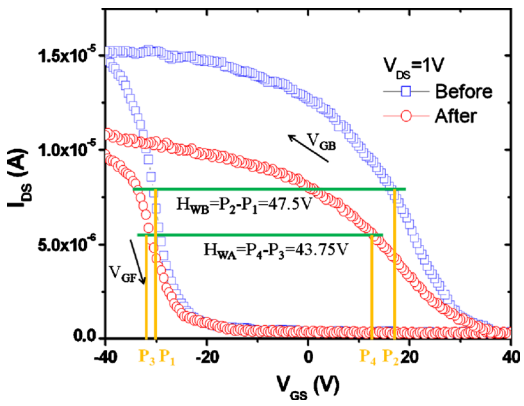

FIG. 2. (Color online) Transfer characteristics of the SWNT TFT measured before and after 1 μm parylene-C deposition measured at V_{DS}=1 V.

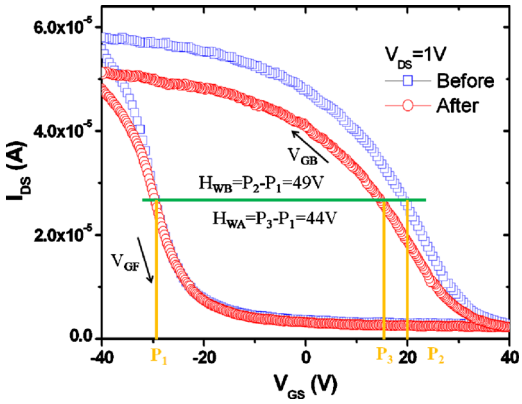

FIG. 3. (Color online) Transfer characteristics of the SWNT TFT measured before and after 3 μm parylene-C deposition measured at V_{DS}=1 V.

based transistors, and it is attributed to charge injection from nanotube at large gate voltages,[14] water molecules,[5] trapped charges at parylene-SWNT interface,[15] other trapped charges from solution processed CNTs[16] (e.g., surfactant, ionic molecules, etc.) and contamination originating during the fabrication of the device.[16] Prior to the deposition of the source and drain electrodes, the parylene-C surface was roughened in an oxygen plasma to improve the adhesion of chromium/gold electrodes. This oxygen plasma treatment breaks the bonds on the parylene surface and induces fixed and mobile charges at the parylene-SWNT interface which can create hysteresis in the CNT FETs.[15] Furthermore, DEP assembly was conducted using nanotubes suspended in deionized water, and both assembly and the I-V study were conducted in atmospheric conditions which all contribute to the observed hysteresis before encapsulation.

For the CNT TFTs with a 1 μm thick parylene-C coating, the two terminal resistance (measured at V_G=−40 V) was increased by 50.3%, whereas the ON current of the device (measured at V_G=−40 V) was reduced by 34.4% from their initial values. The hysteresis width before passivation (H_{WB}) between forward (V_{GF}) and backward (V_{GB}) gate voltage sweep is defined as the difference between P_2 and P_1 (H_{WB}=P_2−P_1), where P_2 and P_1 are backward and forward gate voltages of the TFT and is shown in Fig. 2. The gate hysteresis width before encapsulation was 47.5 V. After the 1 μm parylene-C coating, the transistor showed a gate hysteresis width of 43.75 V (H_{WA}=P_4−P_3). The hysteresis width was reduced by −3.75 V after the deposition of 1 μm parylene-C passivation layer. The change in hysteresis width (ΔH_W) is the difference between the hysteresis width after (H_{WA}) and the hysteresis width before (H_{WB}) parylene-C encapsulation, ΔH_W=H_{WA}−H_{WB}, respectively. The ON/OFF ratio and the threshold voltage (V_{TH}) did not change after the 1 μm parylene-C passivation.

The nanotube transistor encapsulated with a 3 μm thick parylene film displayed a similar electrical behavior as that of the device with a 1 μm thick parylene passivation. Figure 3 displays the transfer characteristics of an SWNT TFT measured before and after the 3 μm thick parylene-C encapsulation. After the 3 μm parylene deposition, the two terminal resistance (measured at V_G=−40 V) of the TFT was increased by 17%, and the ON current of the device was decreased by 13.7% from their initial values, respectively. The TFTs had an H_{WB} of 49 V and H_{WA} of 44 V where the gate

hysteresis width was reduced by −5 V after the 3 μm parylene coating. No significant change in the V_{TH} and ON/OFF ratio was observed after the 3 μm parylene-C deposition.

The changes in the transfer characteristics of TFTs observed in Figs. 2 and 3, such as the increase in the two terminal resistance and the decrease in the on current were caused by the desorption of oxygen molecules from vacuum during polymerization of parylene-C. During the deposition of parylene films, the devices were exposed to low vacuum levels (~2 h and 15 min) where the oxygen molecules adsorbed on the side walls of CNTs were removed. Desorption of oxygen molecules resulted in withdrawal of holes from the CNTs reducing their doping levels and making them less p-type. The reduction in p-doping of SWNTs resulted in a reduction in the channel conductance and a decrease in the ON current of the transistors was observed after their encapsulation with parylene films. In addition, the suppression of water molecules and other trapped charges in vacuum reduced the gate hysteresis widths of these devices but did not fully eliminate them. The parylene coater used in these experiments was PDS2010 which has vacuum levels of about 10^{-3} Torr. The water molecules are very difficult to remove at these low vacuum levels, and their removal requires long annealing times under high vacuum conditions (e.g., 10^{-7} Torr) to further reduce or completely eliminate hysteresis. Lin *et al.*[17] and Kim *et al.*[5] observed similar changes in transfer characteristics and suppression of hysteresis width when nonencapsulated CNT FETs were measured in vacuum. Moreover, other trapped charges from the parylene-SWNT interface, ionic molecules, and surfactants may still be present and could contribute to the remaining hysteresis.

In conclusion, we demonstrated a parylene-C passivation process for encapsulating flexible SWNT thin film transistors and studied the effect of passivation on the electrical properties of these devices. Due to deposition under low vacuum conditions and the desorption of oxygen from the sidewalls of the CNTs there was a slight decrease in the CNT conductance observed from the increase in the resistance and the decrease in the ON current of these devices. Furthermore, parylene-C, being a pin-hole free coating deposited at room temperature may serve to be a promising technology for environmental protection of CNT based devices.

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